AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A surface mount chip package incorporating a semiconductor chip having an integrated circuit, comprising:

a package housing made of a resin that covers the semiconductor chip while avoiding a plurality of conductors extending from the semiconductor chip;

a plurality of external electrodes that are arranged in the package housing in correspondence with a main surface of the semiconductor chip having the integrated circuit and are connected with the plurality of conductors extending from the semiconductor chip, the external electrodes each having a circular shape when viewing the chip package externally in a vertical direction when the semiconductor chip is held horizontally, said external electrodes being arranged in a peripheral area of the main surface; and

at least one marking member that is arranged in the package housing so as to realize a directivity when viewing the chip package externally in the vertical direction, wherein an outline shape of the marking member includes at least one linear portion when viewing the chip package externally in the vertical direction, said marking member being arranged in a central area of the main surface in which no external electrode is arranged.

2. (Cancelled).

3. (Original) A surface mount chip package according to claim 1, wherein the marking member corresponds to a copper post that is arranged independently of the plurality of conductors.

4. (Original) A surface mount chip package according to claim 3, wherein the copper post serving as the marking member has a square shape.

5. (Original) A surface mount chip package according to claim 3, wherein the copper post is covered with a solder layer, a solder print, or a gold bump, thus realizing the marking member.

6. (Original) A surface mount chip package according to claim 5, wherein the marking member has a square shape.

7. (Original) A surface mount chip package according to claim 3, wherein the copper post is increased in size compared with each of the plurality of conductors.

8. (Original) A surface mount chip package according to claim 5, wherein the copper post serving as the marking member is increased in size compared with each of the plurality of conductors, which correspond to a plurality of copper posts.

9. (Original) A surface mount chip package according to claim 6, wherein the copper post serving as the marking member is increased in size compared with each of the plurality of conductors, which correspond to a plurality of copper posts.